



# Contents

## **Preface vii**

## **Chapter 1 Introduction 1**

- 1-1 Circuits in the Hierarchy of Abstractions 1
- 1-2 Digital versus Analog Circuits 3
- 1-3 A Brief History of Digital Scaling 4
- 1-4 Objectives 5
- Summary 6

## **Chapter 2 Digital Logic 7**

- Chapter Objectives 7
- 2-1 Basic Digital Logic 7
  - 2-1-1 Inverter 7
  - 2-1-2 AND/NAND Gate 8
  - 2-1-3 OR/NOR Gate 8
  - 2-1-4 Exclusive OR Gate, XOR/XNOR 8
  - 2-1-5 De Morgan's Laws 9
- 2-2 Physical Implementation of Digital Logic 9
  - 2-2-1 Electrical Digital Circuits 9

- 2-2-2 Inverter Voltage Transfer Characteristic 10
- 2-2-3 Circuits using Ideal Electrical Switches 10
- 2-2-4 Logic Design of NAND and NOR Gates 12
- 2-2-5 Arbitrary Static Digital Gates 13
- 2-2-6 Fan-In/Fan-Out 14
- Summary 15
- Problems 15

## **Chapter 3 The CMOS Inverter 18**

- Chapter Objectives 18
- 3-1 CMOS Devices 18
  - 3-1-1 MOSFET Physical Structure 18
  - 3-1-2 MOSFET Circuit Symbol and Terminal Characteristics 20
- 3-2 MOSFET Device Models for Use in Circuit Design 22
  - 3-2-1 Device Models for nMOSFETs 22
  - 3-2-2 Device Models for pMOSFETs for Use in Circuit Design 24
  - 3-2-3 Small-Signal MOSFET Model 26
  - 3-2-4 Small-Signal Circuit 27
- 3-3 CMOS Inverter Characteristics 27
  - 3-3-1 Voltage Transfer Characteristic 29
  - 3-3-2 Logic Levels and Noise Margin 30
  - 3-3-3 Transient Characteristics 31
- 3-4 CMOS Inverter Analysis 31
  - 3-4-1 Simplified Transfer Characteristic for Hand Calculations 31
  - 3-4-2 Static Analysis of the CMOS Inverter 32
  - 3-4-3 Propagation Delay 35
  - 3-4-4 Power Dissipation 41
- Summary 45
- References 45
- Problems 46
- Design Problems 48

## **Chapter 4 CMOS Logic 49**

- Chapter Objectives 49

- 4-1 Static CMOS Logic Gates 49
  - 4-1-1 Static Characteristics of CMOS Gates 49
  - 4-1-2 Static Analysis of CMOS NAND Gate 50
  - 4-1-3 Transient Analysis of CMOS NAND Gate 53
  - 4-1-4 Transistor Sizing for NAND and NOR 54
  - 4-1-5 Power Dissipation 55
  - 4-1-6 Transistor Sizing for Arbitrary CMOS Gates 56
  - 4-1-7 Internal Parasitic Capacitance 59
- 4-2 Sizing Based on Logical Effort 60
  - 4-2-1 Characteristic Inverter 60
  - 4-2-2 Logical Effort 62
  - 4-2-3 Delay of Paths 65
  - 4-2-4 Optimal Stage Effort 66
  - 4-2-5 Branching paths 67
- 4-3 Dynamic Logic 68
  - 4-3-1 Dynamic Logic—Basic Operation 68
  - 4-3-2 Dynamic Logic Voltage Transfer Function 69
  - 4-3-3 Dynamic Logic Transient Analysis 71
  - 4-3-4 Power in Dynamic Logic 72
- 4-4 Pass Transistor Logic 72
  - 4-4-1 Transistor as a Switch: Passgate 72
  - 4-4-2 Bi-Directional Transmission Gate 73
  - 4-4-3 Pass Transistor Logic 73
  - 4-4-4 Static Operation 75
  - 4-4-5 Transient Operation 75
- 4-5 Sequential Logic 76
  - Summary 80
  - Reference 80
  - Problems 80
  - Design Problems 85

## **Chapter 5 Memory 87**

Chapter Objectives 87

- 5-1 Memory 87
  - 5-1-1 Classification of Memory 87
  - 5-1-2 Memory as Arrays 89

5-2	ROM	91
5-3	SRAM	97
	5-3-1 Data Storage	99
	5-3-2 Write Access	100
	5-3-3 Read Access	104
	5-3-4 Sense Amplifier	110
	5-3-5 Address Decoders and Buffers	111
	5-3-6 Row Decoders	112
	5-3-7 Column Decoders	112
	Summary	112
	References	114
	Problems	114
	Design Problems	116

**Index 117**